A FET-SWITCHED INDUCTION ACCELERATOR CELL*

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Abstract

An array of 24 field-effect transistors (FETs) is being used to switch a nominal 4-kV, 1-μs pulse onto a Metglas induction core at pulse rates exceeding 100 kHz. Each transistor receives isolated gate power from a dc/dc converter and analog pulse control via an optical fiber. The array is part of a specialized circuit architecture that generates bursts of pulses while providing for core reset between pulses. The circuit will accommodate variations in pulse width, repetition frequency (prf), pulse amplitude, burst length and reset interval. The various circuit elements are assembled directly onto the core structure to yield a compact, low-impedance package.

Two prototype machines are presently under development. A 24-FET machine is in operation and capable of 4.2-kV, 1-μs pulses (max.) at a 120-kHz prf for short bursts. Pulse rise and fall times are 25 ns and 65 ns respectively. A 128-FET machine is under construction which should be capable of 6-kV, 1-μs pulses (max.) at a 150-kHz prf for long bursts.

Introduction

Heavy-Ion Fusion

Heavy-ion beams are under study as a future drive source for inertial fusion. In September 1990, a report from the Fusion Policy Advisory Committee (FPAC) endorsed heavy-ion accelerators as the most promising driver for inertial fusion energy [1]. Heavy-ion fusion has been studied in Europe and Japan using rf accelerators [2,3], and in the U. S. using linear induction accelerators [4]. The linear induction accelerator approach is presently being pursued by the Lawrence Berkeley Laboratory (LBL) and by the Lawrence Livermore National Laboratory (LLNL).

As with all large-scale inertial fusion technologies, driver cost is an important consideration when selecting a research pathway. In a study coordinated with LBL, researchers at LLNL have examined a more cost-effective use of induction accelerator technology by proposing a circular configuration of accelerator components, known as a recirculator [5]. A recirculating accelerator yields a system-wide cost savings by having the ion bunch gain multiple use from the expensive capital investments in cells, modulators, and beam-focusing elements. However, the recirculation method requires the cell modulators to operate at a 50- to 100-kHz prf, due to the short ion transit time around the circle. In addition, the modulators must possess great prf agility to keep pace with the increasing ion speed and great agility in pulse width to match the shrinking bunch length.

ILSE Recirculator

The development of high prf, 100-kV induction cell modulators for a commercial fusion driver is a formidable task. We hope to gain insight into the problem by first building a small-scale recirculator consisting of many 5-kV induction cells arranged in a 30-m diameter ring. The proposed small-scale recirculator will accept 10-MeV potassium ions (K+) from a linear accelerator and continue their acceleration to 60-MeV by redirecting the ion bunch around the ring until a final energy is attained. The ions gain speed with each circulation, so the cell prf must also keep pace by increasing from 70 kHz to 200 kHz over a nominal burst length of 100 pulses. The 10-MeV linear accelerator, under development at LBL, is called ILSE (Induction Linac Systems Experiment) and is shown in Figure 1 with the proposed recirculator experiment. Table 1 lists a few of the ILSE specifications along with the pulse requirements for an induction recirculator cell.

Our research is focused on the development of an induction cell and modulator combination that meets the ILSE recirculator requirements in Table 1. Herein, we present data and modeling results from our first device and describe our progress toward a more advanced machine.
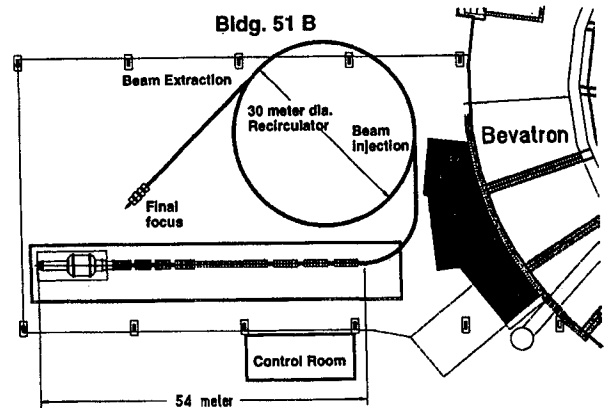
Figure 1. Floor plan of the ILSE accelerator facility showing the recirculator experiment.

Table 1

Accelerator Specifications		Recirculator Specifications	
Mass number	39.1	Initial kinetic energy	10.5 MeV
Charge state	+1	Final kinetic energy	60 MeV
Initial:		Pulse duration	1.0 – 0.4 μs
kinetic energy	2 MeV	Cell voltage	5 kV
pulse duration	1.0 μs	Pulse Rep. Rate	70 – 200 kHz
Final:			
kinetic energy	10.5 MeV	Circumference	100 m
pulse duration	0.4 μs		
beam energy	33 J		
Length of Linac	54 m		

System Issues and Circuit Architecture

Traditional induction accelerator designs separate the functions of cell and modulator into distinct units and interconnect the two by coaxial cables. In a recirculator application, the high cell impedance due to cable interconnections is undesirable because it can lead to a longitudinal instability in the ion beam [6]. The instability issue and the need for pulse format agility led us to merge the functions of cell and modulator into a single low-impedance device. Cost and system efficiency are also important issues that we explored in a tradeoff between initial core costs and magnetic losses. By selecting a well oversized core, we reduced dB/dt and thereby reduced core losses.

We selected the circuit architecture of Figure 2(a) because it generates voltage pulses for acceleration and reset with a single on/off command. When the switch S_1 is closed, the energy storage capacitor
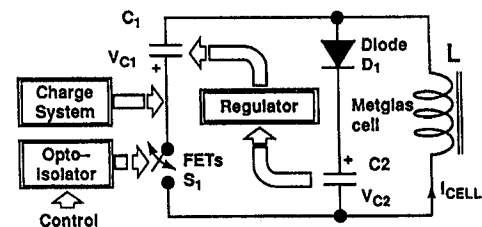

Figure 2(a). Circuit diagram showing switch S_1, energy storage capacitor C_1, and reset capacitor C_2. The regulator controls the voltage on C_2 by returning energy to C_1.

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14. ABSTRACT
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15. SUBJECT TERMS

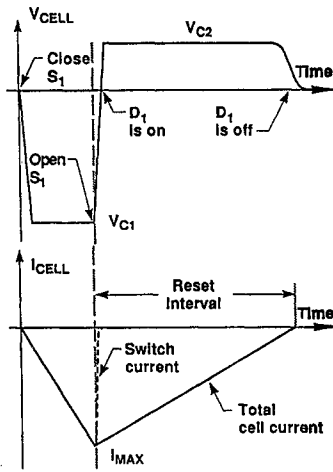| 16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
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Figure 2(b). Idealized cell voltage and cell current waveforms for the circuit in Figure 2(a).

C_1 is connected to the Metglas recirculator cell. Once the acceleration pulse has ended, the switch opens and the cell current is automatically diverted from the switch branch to the reset capacitor C_2, as shown in Figure 2(b). The reset capacitor is precharged to a voltage that dictates the rate of cell current decay and resets the core material by returning the flux density back to its original value. Additional core reset is provided by snubber capacitors across the switch (not shown) and current from the external charging system. The charge system replenishes only a small voltage deficit between pulses because C_1 contains far more energy than the ion beam and core material consume per pulse. The capacitance of C_2 is large compared to C_1 so that the voltage on C_2 increases only slightly from each pulse. Since system efficiency is a key issue, we propose the use of a regulator element that returns the energy recovered by C_2 back to C_1 [7].

FETs were selected as the switching element because they have unique properties: fast rise and fall times, low gate-drive power, low on-state impedance, and a capacity for high prf operation. These FET characteristics make series and parallel switch configurations easy to design and very effective in high prf applications [8]. We arranged our FETs into a series-parallel array of independent switching circuits, where each circuit is powered by a dc/dc converter and commanded on and off by a fast optical link. Our earliest switching system consisted of only four circuits (two in series by two in parallel) that switched 1 kV onto a 2605S-3A Metglas core [9]. Our latest machine surrounds the same Metglas core with 24 independent switching circuits by stacking six switches in series and connecting four switch stacks in parallel. We call this switching configuration our 6 x 4 machine.

6 x 4 Machine Performance

Figure 3 is a simplified network diagram of the 6 x 4 machine showing the four energy storage capacitor banks, four reset circuits, and the four switch branches. The circuit elements in Figure 3 are grouped around the core in four quadrants, as shown in Figure 4.
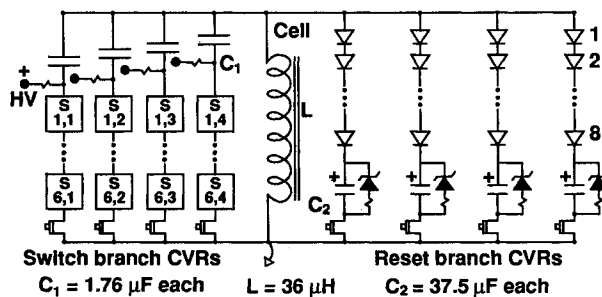

Figure 3. Network diagram for the 6 x 4 machine. Each switching element is a circuit card containing a single FET, gate driver, optical receiver, and a power converter.
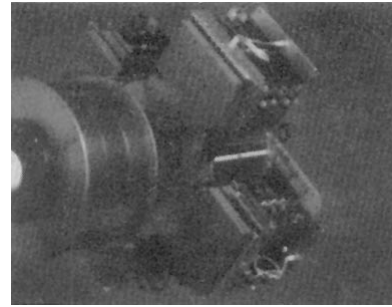

Figure 4. Photograph of the 6 x 4 machine showing the induction core and switch stacks.

There is no energy recovery system on this machine, so the reset capacitor voltage is controlled by an external power supply and regulated by zener diodes. Switch stack voltage and cell voltage are both measured using high-impedance probes, while the switch and reset currents are measured using eight, 50-mΩ current-viewing resistors (CVR).

A digitized record of a single switch stack voltage, four switch currents and four reset currents are all shown in Figure 5 (a) through (c).
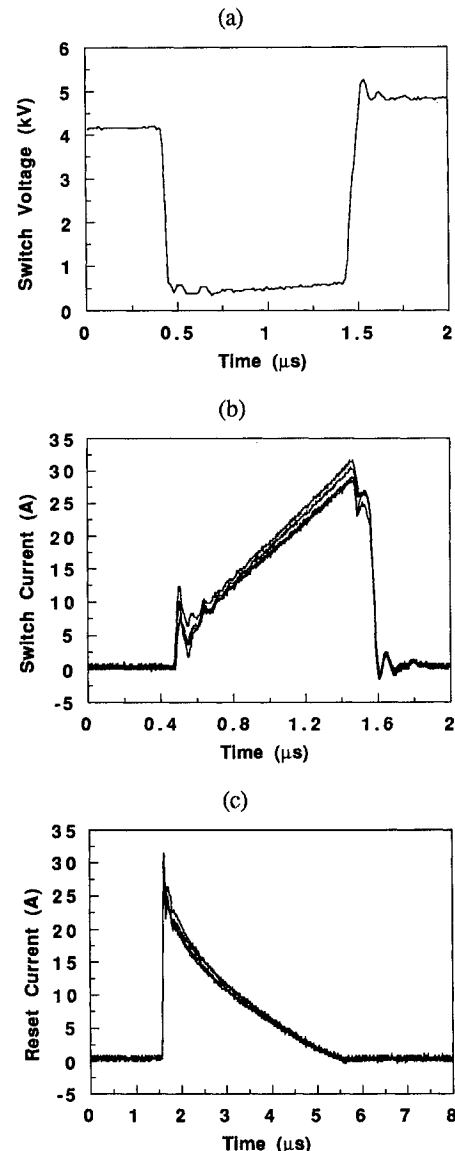

Figure 5. (a) One of four switch stack voltages. (b) Overlay of four switch branch currents. (c) Overlay of four reset branch currents.

The superimposed current data indicate good current sharing between the various switch and reset branches due to precise switch timing and and similar on-state resistances. The measured cell voltage is shown in Figure 6 along with the total cell current, which is a computer summation of all the switch and reset currents from Figure 5. The small voltage spike at the start of the reset interval is due to the reset circuit inductance.
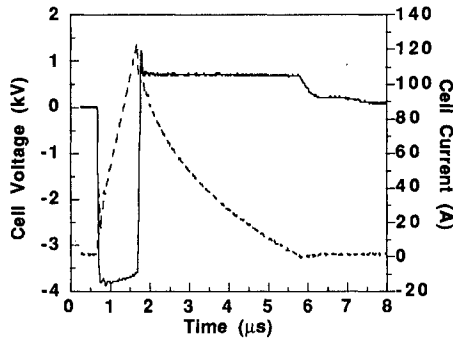

Figure 6. Cell voltage (solid line) and total cell current (dashed line).

An illustration of pulse width agility is shown in Figure 7(a) for two pulses with different widths but a constant reset voltage. Similarly, Figure 7(b) shows a two-pulse change in reset voltage for a constant pulse width.
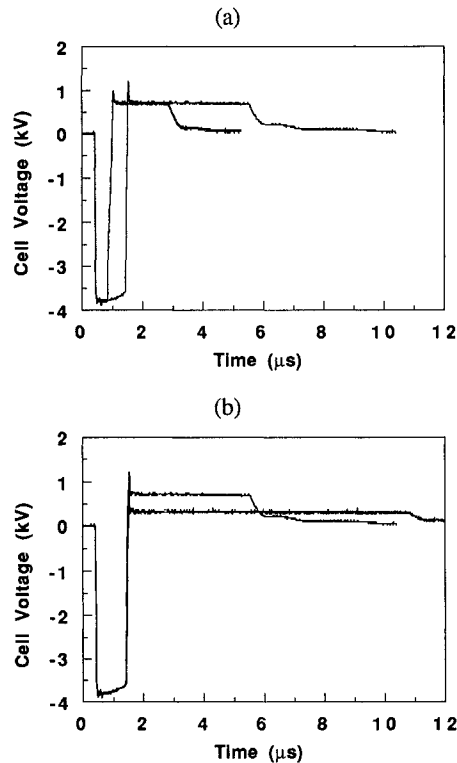
(a)

(b)

Figure 7. Comparison of reset intervals for two pulses: (a) A 400-ns pulse and a 1-µs pulse are compared for a constant reset voltage of 700 V. (b) Two 1-µs pulses are compared with reset voltages of 700 V and 300 V.

One should note that variations in pulse width or reset voltage are automatically matched by a shift in the reset interval. Consequently, the acceleration and reset pulses have equal volt-second products. Figure 8 shows the cell voltage during a five-pulse burst at a 100-kHz prf. The energy for all five pulses is supplied by a single charge from the core-mounted capacitor banks.
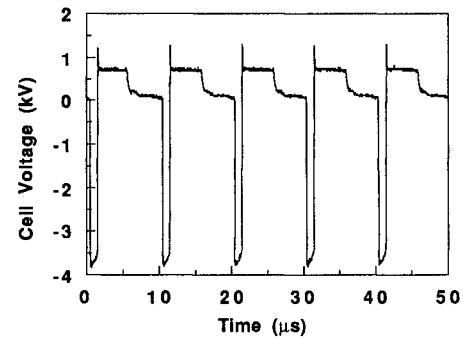

Figure 8. Cell voltage record for a five-pulse burst of 1-µs pulses with a pulse separation of 10 µs (100-kHz prf).

A safe operating area for the machine is primarily determined by the FET array limitations for breakdown voltage and pulsed current. The array current limit can be reached by an excess of either pulse width or charge voltage. The array breakdown voltage may be exceeded by the sum of the charge voltage, reset voltage, and any pulse overshoot. The maximum prf is operationally limited by restricting the pulse width and reset interval combination to be less than the burst period.

PSpice Modeling

We selected PSpice to assist us with the 6 x 4 machine analysis and to assess the next generation of machine designs. We were especially interested in tracing the flux density behavior in the 6 x 4 machine core to determine if the reset circuit provided an open or closed flux cycle. The magnetic simulation parameters in PSpice were adjusted to match both small-core test data and an empirical equation that best fit available test data in the literature [10]. A single-pulse comparison of simulation and measured data is shown in Figure 9. A multipulse simulation of the core's B-H loop trajectory is shown in Figure 10.
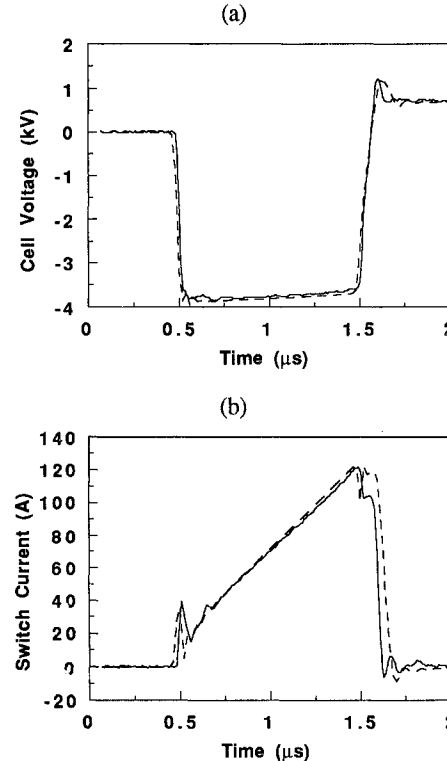
(a)

(b)

Figure 9. Single-pulse comparisons between measured data (solid line) and PSpice simulations (dashed line): (a) Cell voltage. (b) Switch current for all four branches.
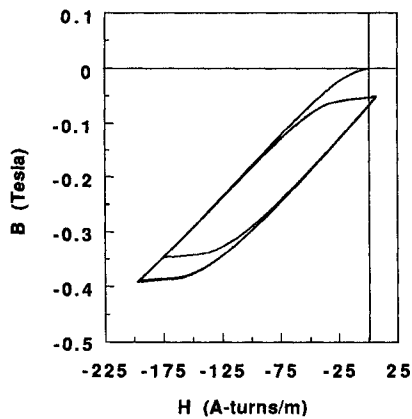
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Figure 10. Plot of the core's magnetic flux density (B) vs magnetic field intensity (H) for a four-pulse simulation.

The loop simulation starts at the B-H origin to illustrate that the network provides a stable reset condition after a few pulses. More information is available about our modeling effort from Ollis, *et al.*, in these proceedings [11].

Next Generation Machine

Plans for our next induction cell include increases in cell voltage and power-handling capacity with decreases in machine size and cost per kilowatt. The recirculator specifications for voltage and burst duration require our new induction cell to exceed a 5-kV cell voltage and to be powered from a large external capacitor bank. The new machine will also be smaller than the 6 x 4 machine by using one third less core material and surface-mount electronics for the gate drive circuits. We plan to increase the new machine's peak and average power capacities while lowering the system cost per kilowatt by using 32 power converters and optical links to serve 64 gate drive circuits. Similarly, each gate drive circuit commands two power FETs in parallel to yield a total of 128 FETs. The general circuit architecture remains the same as the 6 x 4 machine, but this new device places eight parallel modules around a smaller core with eight series switching elements per module. We call this array configuration our 8 x 8 machine and list its electrical specifications in Table 2.

Table 2

Electrical Specifications

Total machine capacitance	4.8 μF (four banks)
Cell inductance	24 μH
Peak cell current @ 1 μs, 5 kV	208 A
Maximum:	
stored energy	86.4 J
charge voltage	6 kV (capacitor limit)
array voltage	8 kV (FET stack limit)
array current	670 A (pulsed)
Minimum:	
pulse separation	6.67 μs (150 kHz)
reset interval	5 μs

Summary and Conclusions

We developed a compact cell and modulator combination that generates 4-kV, 1-μs pulses onto a Metglas induction core at pulse rates exceeding 100 kHz. The solid-state circuit architecture has an ability to power an all-inductive load, freely vary pulse width and prf,

and provide for cell reset between pulses. PSpice models have also been developed and show a reasonable agreement with measured data. Construction is underway on a new device that will yield higher cell voltages and pulse rates.

We believe our FET-switched device is a good example of smart power management applied to a pulse power problem [12]. In this context, a "smart" pulse power system can adapt to rapidly changing load conditions because the advanced switching technology can communicate with a computer-based control system. Smart power management is required for heavy-ion recirculators and we believe it also applies to other industrial applications where small size, reliability, efficiency and low cost are prime issues.

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